

AMENDMENTS TO SPECIFICATION

Page 1, line 1 to Page 2, line 4:

When the current passing through the bipolar junction transistors (BJT) Q1 and Q2 is equal to each other, by means of the transistors M5 and M6, the voltages of the nodes N5 and N6 are equal to each other. When the size of the BJT Q2 is larger than that of the BJT Q1, and the voltages of the node N6 and N5 are equal because of the cascode current mirror, a first current directly proportional to the surrounding temperature will be outputted from the transistor M7 and M8. Because the emitter-base voltage of the BJT Q3 is inversely proportional to the surrounding temperature, a reference voltage VREF1 irrelevant to the surrounding temperature will be generated when the first current ~~passing~~ passes through the resistance R2 and bipolar junction transistor Q3.

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Therefore, the main objective of the present invention is to provide a bandgap reference circuit for generating a low reference voltage. The bandgap reference circuit of the present invention uses serially connected resistances and an operational amplifier of which an input differential pair is ~~a-an~~ N-type metal oxide semiconductor (MOS) so that the bandgap reference circuit can operate under a low voltage.

Page 3, line 22 to Page 4, line 6:

The present invention relates to a bandgap reference circuit for generating a reference voltage. The bandgap reference circuit comprises an operational amplifier comprising a first and a second input ends and an output end; a plurality of transistors connected to the operational amplifier; a plurality of resistances connected to the plurality of transistors; and a plurality of bipolar junction transistors separately connected to the plurality of resistances. A ~~first~~ First and a second resistances of the plurality of resistances are used for voltage level shifting so that the operational amplifier with N-type input ~~transistor~~ transistors can normally operate.

Page 6, lines 12-19:

As shown in Fig. 3, the operational amplifier 32 comprises a first and a second input ends 34, 36, and an output end 38. The first input end 34 is connected to the drain of the transistor M17, the second input end 36 is connected to the drain of the transistor 18, and the output end 38 is connected to the gates of the transistors M17, M18, M19. Besides, one end of the resistance R3 is connected to the first input end 34 of the operational amplifier 32, and the resistance R4 is connected to the second input end 36 of the operational amplifier 32.